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# STUDY OF 600 V-CLASS SUPERJUNCTION METAL–OXIDE–SEMICONDUCTOR FIELD-EFFECT TRANSISTORS WITH TERMINATION OF TRENCH STRUCTURE AND SIPOS

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***ABSTRACT***

***The terminal structure of the traditional Superjunction Metal–Oxide–Semiconductor Field-Effect Transistors (SJ-MOSFETs) requires individual designs and consumes a large area due to the different parameters of the base materials. Therefore, this paper proposes a terminal structure, which is also a superjunction, where semi-insulating polycrystalline silicon (SIPOS) is deposited on the P-pillar of the external Trench. As terminations have the N-type and P-type dosage concentrations the same as cells, it is a relatively simple in design. Under the condition of maintaining the breakdown voltage of SJ-MOSFETs at 600 V-class, the terminal structure proposed in this paper can reduce the area by more than 29%, as compared with the traditional terminal structure.***

***KEYWORDS: SJ-MOSFETs, Termination, SIPOS, Trench & Specific On-Resistance***

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Original Article

## INTRODUCTION

### Background

Power metal-oxide-semiconductor field-effect transistors (MOSFETs) have been continuously developed to promote block ability and decrease power loss through the progress of fabrication technology and the evolution of device structures [1]. Previous studies show that, through the improved power of MOSFETs, including lateral, vertical, and the design adopting the concept of reduced surface field (RESURF) and superjunction (SJ), devices show better operational characteristics regardless of manufacturing on a Si wafer or SOI [2,3]. SJ devices create a high breakdown voltage by controlling the charge balance and low on-resistance beyond the Si-limit by high doping in the conduction region [4]. In 2008, J. Sakakibara et al. reported that a SJ-MOSFET with a trench gate and high aspect ratio P/N columns structure is meant to obtain low on-resistance, which is lower than that of IGBTs [5]. T. Tamaki et al. promoted the 600 V-class SJ-MOSFETs by using a tapered sidewall trench [6]. For 600 V-class devices, the specific on-resistance of SJ-MOSFET is one fifth that of a conventional VDMOSFET. However, designing a superjunction structure is difficult, and requires a large area to obtain a high blocking voltage, which leads to increased cost.

The parallel diffusion technique is often used in power devices. The junction is formed by diffusion and ion implantation; however, as the impurities diffuse laterally, the level of lateral diffusion is 85% of the vertical. Thus, if the junction is designed as a square window, it will form a cylindrical or spherical junction. The electric field is uniform in the interior of the junction, and its breakdown voltage (BV) is the same as that of a parallel junction; however, at the edge, the electric fields gather inseparably close due to the cylindrical or spherical junction, thus, causing a smaller breakdown voltage than that of a parallel junction. The area of an actual device is

not infinitely fabricated, and the parallel junction must be terminated at the edge to create a bow junction. Therefore, as the design of a termination junction is to make the distribution of the termination's electric field like a parallel junction, it extends the electric field to any region in the silicon substrate [7].

The traditional floating ring termination can bear high voltage only with a larger structure area. The previous paper (Ref 8) proposed combining semi-insulating polycrystalline silicon (SIPOS) with a P- junction to effectively reduce the termination area [9, 10]. This paper applies this concept in a superjunction, i.e. to design a termination with trench and SIPOS, and thus, achieve a simple design while reducing the consumption area, without increasing the procedures or steps. SIPOS winds and covers the P-pillar external trench in the form of a paper clip, in order that the P-pillar trench is connected in series through SIPOS.

## METHODS

First, SJ-MOSFETs with over a 600 V reversed bias were studied by simulation. As there is a difference in the device structure of a simulation device and a fabricated device, this study specifically blocked the voltage of the simulated devices at 700 V in order to increase manufacturing potential. The thickness of the used N-type epitaxial layer (EPI) was 45 um, and three concentrations were considered, $7.5\times10^{14}$, $9\times10^{14}$ and $1.1\times10^{15}$ $cm^{-3}$. The cell structure is displayed in Figure 1. The following is a series of optimized simulations by the Silvaco Simulator for PNPN and SIPOS termination, including the depth, width, interspace, and number of the trenches in the termination, for the 700 V-class BV. During actual production, SIPOS is wound and covered on the P-pillar trench in the form of a paper clip. However, as the Silvaco Simulator cannot provide 3D structural simulation, this paper adopted 2D structural simulation, SIPOS was directly deposited on all trenches, and a very thin p-ring was arranged between the trenches to connect them, as illustrated in Figure 2. Finally, the fabrication of SJ-MOSFET with SIPOS termination was realized and the key processes are as follows: Step 1: growth of one N-type epitaxial layer on an N-type substrate with a thickness of 45 um; Step 2: JFET phosphorus dose with $2\times10^{12}$ $cm^{-2}$ and thermal drive-in; Step 3: P-base boron doping with $7\times10^{13}$ $cm^{-3}$ and thermal drive-in; Step 4: defining of the guard ring required for the termination structure; Step 5: etching of 37 um-depth trench and filling the P-type epitaxial, then, polishing the surface using Chemical Mechanical Polishing, CMP; Step 6: deposition of one oxide layer with a thickness of 9000 Å on top of the epitaxial layer; Step 7: Sacrificial Oxidation process, then growth of one gate oxide with a thickness of 1000 Å; Step 8: deposition of polysilicon with a thickness of 4000 Å and define the gate and SIPOS; Step 9; arsenic doping for N+ source and annealing process with an $N_2$ purge for damage repair and dopant activation; Step 10: deposition of one layer of BPSG by CVD, then surface polishing using chemical mechanical grinding to create an ILD dielectric layer; Step 11: aluminum deposition as the source electrode after etching of ILD.

## RESULTS

### SJ-MOSFET Optimized Simulation

The maximum BV decreases when the concentration of the epi-layer increases and the corresponding concentration of the P-pillar increases. According to the simulation results shown in Figure 3, when a device with a rating blocking voltage of 700 V is to be obtained, the concentration of the P-pillar must be between $2.1\times10^{15}$ and $4.7\times10^{15}$ $cm^{-3}$. The concentrations of the epi-layer are $7.5\times10^{14}$ and $9\times10^{14}$ $cm^{-3}$, and their corresponding simulated specific on-resistance are 43 and 36.17 $m\Omega\text{-}cm^2$. Thus, the simulations used concentrations of epi-layer and P-pillar at $9\times10^{14}$ and $3\times10^{15}$ $cm^{-3}$.

**SJ-MOSFET Termination Optimized Simulation**

- **Trench Width**

In order to achieve the rating of a 700 volt breakdown voltage, the trench width of the SJ-MOSFET must be simulated. In Figure 2, the epitaxial thickness is 45 um, the concentration of the P-type trench is fixed at $3\times10^{15}$ $cm^{-3}$, the number of trenches is set at 7, and the P-type trench widths are modulated from 1 to 7 μm in order to obtain the breakdown voltage, which is defined as the reverse current to 1 nA/μm. The simulation results are as shown in Figure 4. When the width is greater than 5 um, it causes a breakdown voltage decrease because the P-type trench area is not fully depleted.

- **Trench Depth**

The next simulated parameter is a trench area depth with a fixed trench concentration of $3\times10^{15}$ $cm^{-3}$ and a width of 5 μm. The P-type trench depth was modulated from 0 to 45 μm, and the breakdown voltages were obtained, as seen in Figure 5. The results show that when the P-type trench depth is great, the electric field can effectively extend downward promoting a breakdown voltage. However, the breakdown voltage has a direct relationship to the epitaxial layer's thickness, thus, the epitaxial layer's thickness must be thick (we used 45 um), and the trench depth must be deeper than 33 μm to obtain a breakdown voltage of over 700 V. Therefore, the depth of the P-type trench area was set at 37 μm, and the aspect ratio (A/R) was 7.4 in accordance with the specifications of a breakdown voltage of 700 V.

- **Trench Interspace**

The following optimizes the distance between trenches varying from 2 μm to 14 μm, and the simulation results are as shown in Figure 6. Through modulation, it can be observed that the long interspace of a P-type trench will affect the electric field's outward extension, thus, creating an N-type and P-type carrier imbalance, and causing the breakdown voltage to decrease. Therefore, the interspace of the P-type trench area is set at 10 μm.

- **Trench Number**

Our final simulation is the trench number, where the concentration, width, and depth of the P-type trench interspace are 3×1015 cm-3, 5 μm, 37 μm, and 10μm, respectively. The P-type trench numbers were 3, 4, 5, 6, 7, 8, 9, 10, and 11 to simulate the breakdown voltage, and the results can be observed in Figure 7. When the number of P-type trenches was increased to over 6, the breakdown voltage did not have the ability to increase, as the vertical distribution of the electric field did not extend to the trenches that were far away from the source. Obviously, when there are over 5 P-type trenches, the performance characteristics for the breakdown voltage have no significant effect. Table 1 shows the simulation results of SJ-MOSFETs using 5 and 7 trenches in the termination. While they have the same cell breakdown voltage and specific on-resistance, they have different termination breakdown voltages and lengths due to the number of trenches. Devices with 5 trenches could reduce the consumed area (105 um termination length) and withstand voltages over 700 V.

- **Charge Balance**

When the P-type concentration and N-type concentration of column zone of the superjunction component fully achieve mutual supplementation, the component has the best withstand voltage performance. Therefore, whether the PN concentration of a column zone matches will decide the size of the breakdown voltage. Analysis of the relation between

charge imbalance and withstand voltage can help us understand the tolerable concentration variance of the PN column zone during actual component production. The following shows the dosage concentration simulation of the P-type at N-type concentrations of $7.5\times10^{14}$ $cm^{-3}$, $9\times10^{14}$ $cm^{-3}$ and $1.1\times10^{15}$ $cm^{-3}$ respectively. The calculation formula of the charge imbalance percentage is, as follows:

$$\text{Charge imbalance (\%)} = \frac{(Q_P - Q_n)}{Q_n} \times 100\%$$

Wherein

**Qp:** charge concentration of P-type column zone

**Qn:** charge concentration of N-type column zone

From the curve diagram of the relation between charge imbalance percentage and breakdown voltage in Figure 8(a), it can be known that, when the concentration of the N-type zone is higher, the reduction of the breakdown voltage caused by the charge imbalance will be more significant. To maintain the breakdown voltage at 700 V, when the concentration of the N-type zone is $7.5\times10^{14}$ $cm^{-3}$, the tolerable imbalance percentage is about ±20%; when the concentration of the N-type zone is $1.1\times10^{15}$ $cm^{-3}$, the tolerable imbalance percentage decreases to ±15%. Thus, it can be seen that the charge imbalance has serious influence on breakdown voltage. Figures 8(b) and 8(c) show the voltage withstand simulation diagram under the charge balance percentage and the charge imbalance percentage of 50%, respectively, when the concentration of N-type zone is $1.1\times10^{15}$ $cm^{-3}$. The diagrams show that, when the concentration of the P-type zone increases to 50%, the P-type column zone cannot reach full depletion, which causes the breakdown voltage to reduce from 772 V to 460 V.

## DISCUSSIONS

Depositing a SIPOS between the two ends of the electrodes can obtain more uniform electric potential distribution. Figures 9 and 10 respectively show the equipotential distribution diagrams with and without SIPOS, where the breakdown voltage of the terminal structure without SIPOS is only 600 V. Obviously, connecting the trenches through SIPOS can effectively improve potential distribution and the voltage withstanding.

Another important point is to allow the breakdown point to take place evenly in each trench during the termination design. The analysis diagrams of the simulation results with and without SIPOS are shown in Fig. 11 and 12. Figure 11 displays a uniform distribution of the impact generation rate. Thus, an actual device can be blocked at high voltage and more stable operation.

### Measurements

The measured and simulated diagrams of the breakdown voltage under different epitaxial concentrations, P-pillar doping, and with a 5 um trench width, 37 um trench depth, 10 um trench interspaces, and a 140 um termination length (7 trenches) are as shown in Figure 13, where the curves with solid and hollow symbols are the corresponding simulated and measured results, respectively. When the N-type epitaxial layer has a higher dosage concentration, the P-type column zone requires a higher dosage concentration to achieve a charge balance and make the electric field stretch to the drain end of the components. Figure 14 shows the original diagram corresponding to the breakdown voltages for the measurements

and simulation with the concentration of epitaxial and P-pillar at $9\times10^{14}$ and $3\times10^{15}$ $cm^{-3}$, respectively. The experimental results also validate the feasibility and reliability of the simulation of this paper. Table 2 shows a series of measurements, including specific on-resistance (Ron,sp), input capacitance (Ciss=Cgd+Cgs), figure of merit (FOM), and breakdown voltage (BV), for three different epitaxial concentrations. The turn-on resistance of this paper is higher than that of the superjunction power transistor on the market because the processes used in this experiment is not in the high stage, the cell has its limitation in design. Therefore, FOM is small when the epitaxial concentration is high, meaning devices have good operative efficiency because more N-type carriers of the PN junction can promote a decrease in on-resistance and input capacitance.

## CONCLUSIONS

This paper introduced SJ-MOSFETs with a termination structure utilizing SIPOS wrapped on the P-pillar trench. Compared with the traditional structure, the design concept of this termination can reduce the area of termination in the same grade of breakdown voltage. For example, the planar high-power MOS transistors TOSHIBA TK6A65D with a withstand voltage of 650 V, its termination is about 180 um long. If the terminal structure in this paper is used, it is possible to reduce 29% of area loss under the condition of maintaining the same electric characteristics. Figure 15 displays the relationships between Ron, sp, and BV for different power devices, including DMOS and SJ-MOSFETs, with various A/Rs [5].

**Table 1: Simulation of SJ-MOSFETs with 5 and 7 Trenches in the Termination**

| | 5-Trench Termination | 7-Trench Termination |
|---|---|---|
| EPI Concentration ($cm^{-3}$) | $9\times10^{14}$ | $9\times10^{14}$ |
| P-pillar Concentration ($cm^{-3}$) | $3\times10^{15}$ | $3\times10^{15}$ |
| Cell Breakdown Voltage (V) | 756 | 756 |
| Cell $R_{on,sp}$ $V_G$=10V(mΩ-$cm^2$) | 36.17 | 36.17 |
| Termination Breakdown (V) | 710 | 776 |
| Termination Length (um) | 105 | 140 |

**Table 2: Characteristics of Fabricated SJ-MOSFETs with Various Epitaxial Concentrations**

| EPI Conc. ($cm^{-3}$) | Ron,sp (mΩ-$cm^2$) | Ciss (pF) | FOM (mΩ-$cm^2$-pF) | BV (V) |
|---|---|---|---|---|
| $1.1\times10^{-15}$ | 29.00 | 1828 | $5.30\times10^4$ | 626 |
| $9\times10^{-14}$ | 36.67 | 1813 | $6.65\times10^4$ | 656 |
| $7.5\times10^{-14}$ | 42.10 | 1798 | $7.57\times10^4$ | 679 |

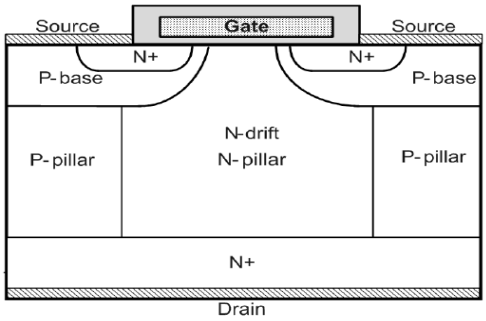



**Figure 1: Cell structure of SJ-MOSFET**

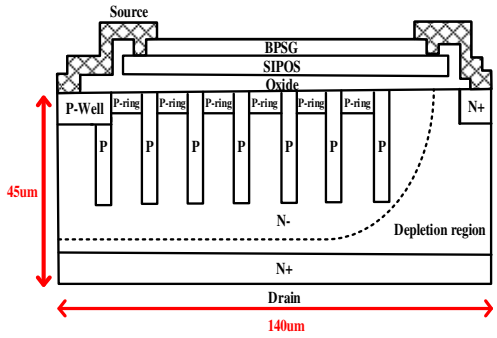



**Figure 2: Schematic Structure of SJ-MOFET Termination with SIPOS**

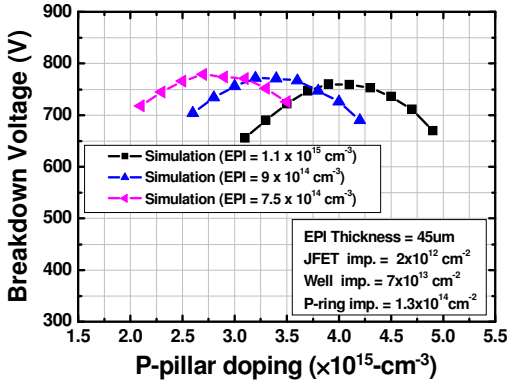



**Figure 3: Diagram of Breakdown Voltage Simulation Based on Three Concentrations of P-pillar**

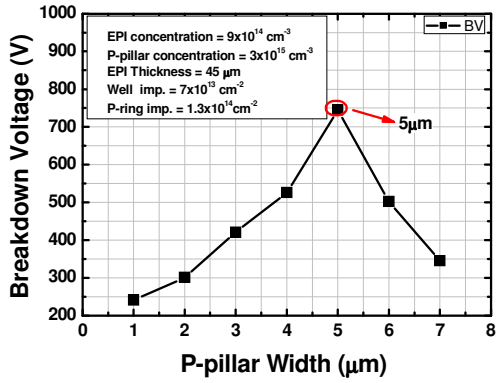



**Figure 4: Relationship between the P-Pillar Width and Breakdown Voltage**

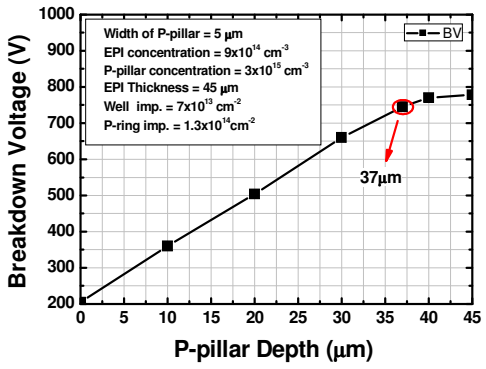



**Figure 5: Relationship between the P-Pillar Depth and Breakdown Voltage**

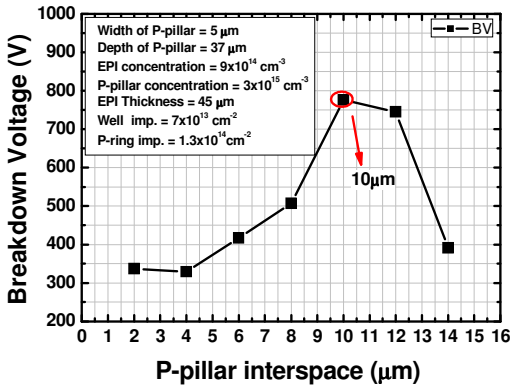



**Figure 6: Relationship between the Interspace of the P-Pillar and Breakdown Voltage**

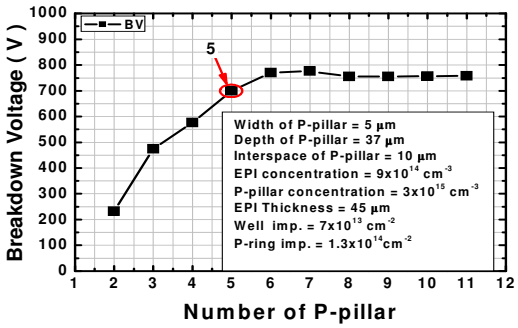
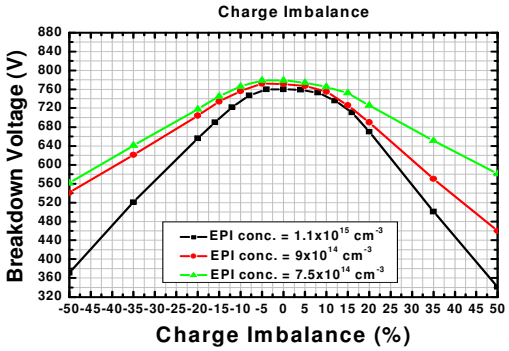
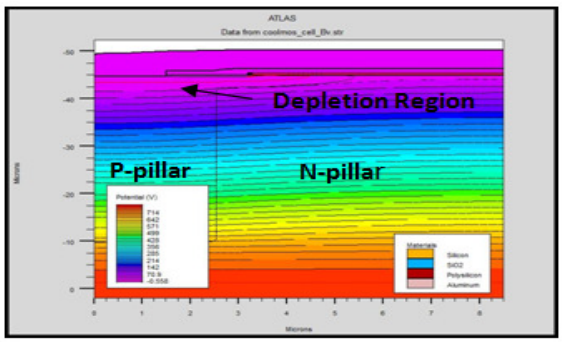


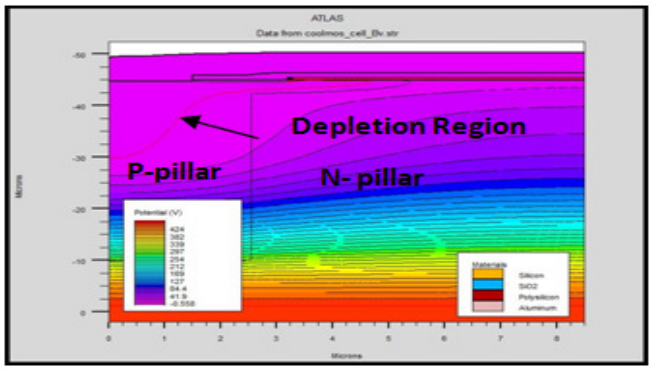

**Figure 7: Relationship between the Number of P-pillars and Breakdown Voltage**




(a)




(b)




(c)

**Figure 8: (a) Simulation Curve Diagram of SJ-MOSFET Withstand Voltage to Charge Imbalance (b) Distribution Diagram of Equipotential Line and Depletion Area during SJ-MOSFET Charge Balance (c) Distribution Diagram of Equipotential Line and Depletion Area during SJ-MOSFET Charge Imbalance (50%)**

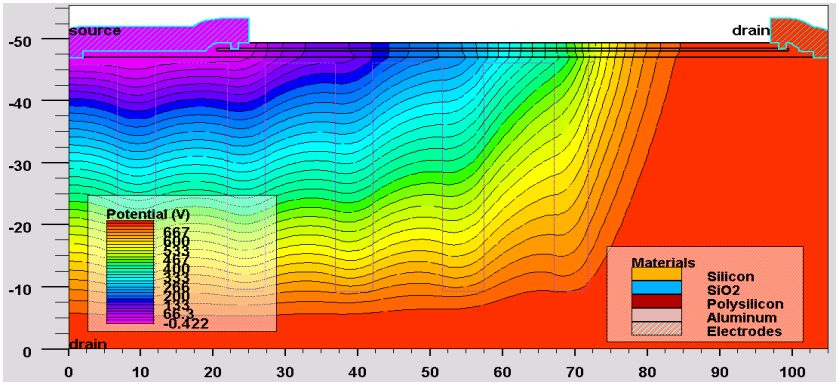



**Figure 9: Diagram of Equipotential Simulation of SJ-MOSFET Termination with SIPOS Structure**

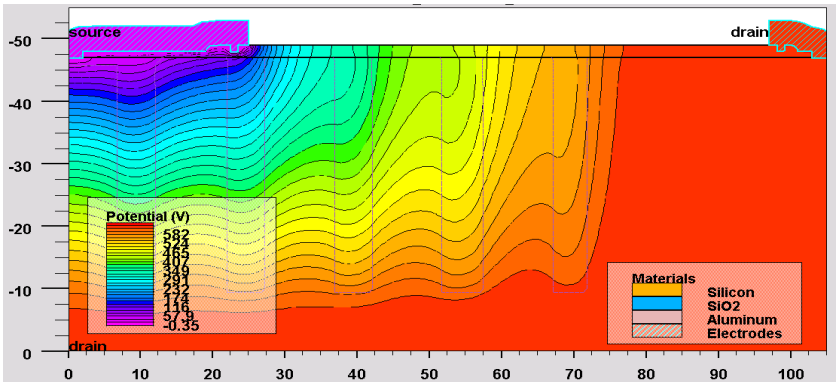



**Figure 10: Diagram of Equipotential Simulation of SJ-MOSFET Termination without SIPOS Structure**

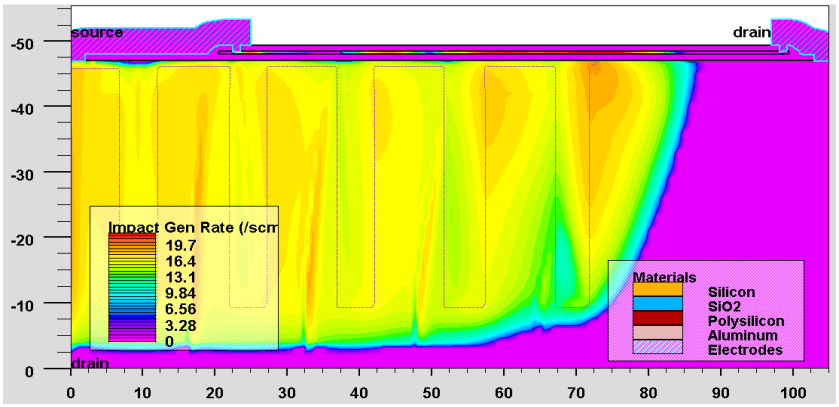



**Figure 11: Breakdown Point Simulation of SJ-MOSFET Termination with SIPOS Structure**

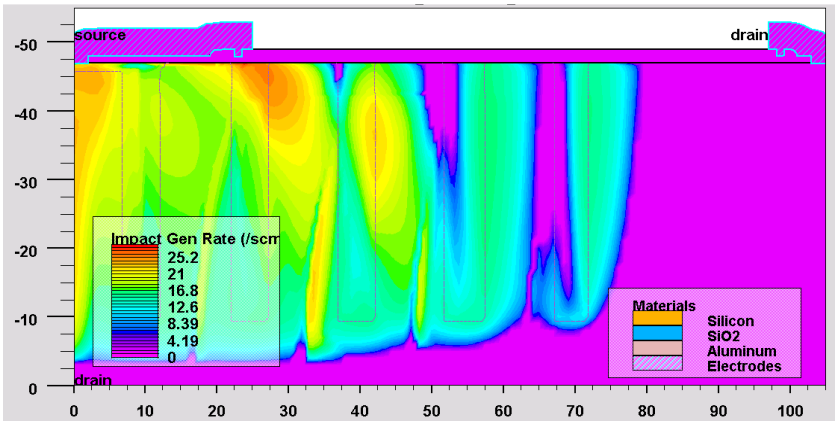



**Figure 12: Breakdown Point Simulation of SJ-MOSFET Termination without SIPOS Structure**

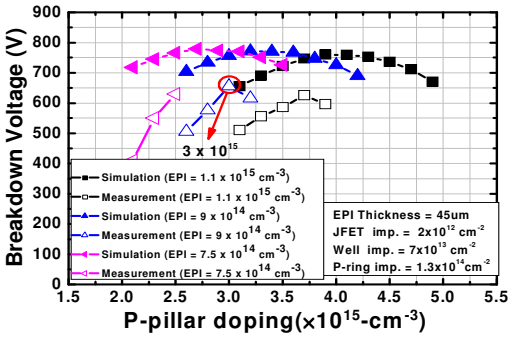



**Figure 13: Diagram of Breakdown Voltage Measured and Simulated Based on Different Concentrations of P-Pillar**

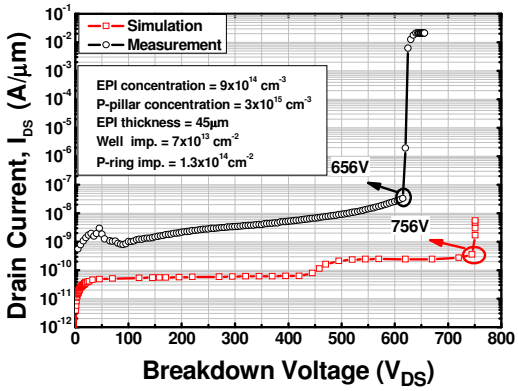



**Figure 14: Original Diagram Corresponding to the Breakdown Voltages for the Measurement and Simulation with the Concentration of Epitaxial and P-pillar at $9\times10^{14}$ and $3\times10^{15}$ $cm^{-3}$, Respectively**

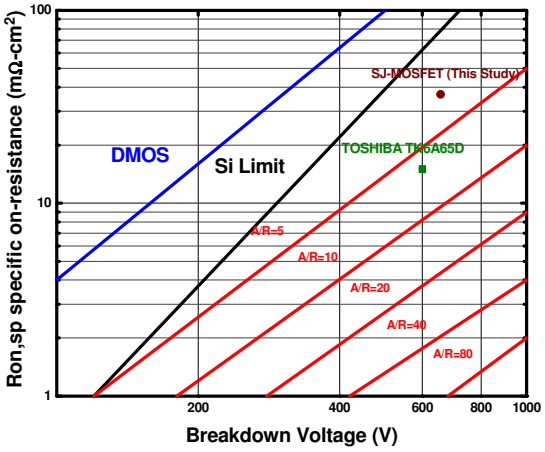



**Figure 15: Relationship between $R_{on,sp}$, and Breakdown Voltage of Power Devices**

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